# An X- to Ku-Band 3-Bit Digital MEMS Varactor

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***Abstract*—A 3-bit digital microelectromechanical system (MEMS) varactor bank is demonstrated on a low-cost glass substrate. It is composed of three discrete-position varactors, each of them achieving a capacitance ratio close to 3 : 1. The total capacitance of the varactor bank is tunable from 146 fF to 430 fF in eight states and is suitable for X- or Ku-band operation. The design can be easily scaled to Ka-band frequencies.**

***Index Terms*—Capacitor, microelectromechanical system (MEMS), micromachining, microwave, millimeter-wave, switch, varactor.**

## I. Introduction

MICROELECTROMECHANICAL system (MEMS) varactors with analog tuning have seen limited developments mostly because of their low capacitance ratio of 1.25–1.35 [1]. A solution with separate electrodes and a nonplanar membrane has been developed by Zou *et al.* [2] and Dussopt *et al.* [3] and resulted in an analog capacitance ratio of 1.7–1.9. Another solution presented by Brank *et al.* [4] employs an array of MEMS switched capacitors. A limitation of this design arises when two separate components are used for the MEMS switch and the MIM capacitor, resulting in a large physical size and a parasitic inductance and resistance associated with their interconnection.

The digital varactor and varactor bank presented in this paper uses a device previously developed at the University of Michigan [3] combining the functions of a MEMS switch and a metal–air–metal (MAM) capacitor. This component has a small size and provides very low losses due to the MAM configuration (no insulating dielectric) and therefore is very suitable to microwave and millimeter-wave applications.

## II. Discrete-Position Varactors: Design, Fabrication, and Measurements

The discrete-position varactor design consists of a nonplanar membrane over a CPW line. The membrane is actuated by two electrodes located in the slots of the CPW $t$-line. The membrane is fabricated so that its height in the center ($g_1 = 1.5\ \mu$m) is larger than its height above the electrodes ($g_2 = 1\ \mu$m). This shape preserves an air gap between the CPW center conductor and the membrane when the bridge is pulled in the down-state position. Hence, this varactor achieves two capacitance values: $C_u = \epsilon_0 W w/g_1$ in the up-state position and $C_d = \epsilon_0 W w/(g_2 - g_1)$ in the down-state position. The theoretical capacitance ratio is $C_r = C_d/C_u = g_1/(g_2 - g_1)$, neglecting the fringing capacitance. In practice, the capacitance ratio depends on the planarity of the membrane. The varactors presented in [3] achieved a capacitance ratio $C_r = 1.87$, while it is $C_r \approx 3$ ($g_1 = 1.5\ \mu$m, $g_2 = 1\ \mu$m) in this work.

The discrete-position varactor is fabricated on a 20-mil thick glass substrate with $\epsilon_r = 4.6$ (Fig. 2). The CPW transmission line dimensions are 80/160/80 $\mu$m (77 $\Omega$), and the electrodes and bias lines are composed of 1200 Å-thick sputtered SiCr, with a measured resistivity of 1000 $\Omega/$ sq. The electrodes are covered by 2000 Å of $Si_xN_y$ deposited by PECVD. The CPW lines are defined using a lift-off technique with evaporation of Ti/Au 500/5000 Å. The sacrificial layer is PMMA, partially etched over the electrodes using an $O_2$ plasma RIE process to achieve the two different heights. The bridge is fabricated by sputtering 0.8 $\mu$m of gold and electroplating 2 $\mu$m over the anchors and over the steps of the membrane. The electroplating locally stiffens the nonplanar membrane, and reduces the deformations due to the steps. Finally, the sacrificial layer is etched in PRS 2000 (wet-etch) and the bridges are released in a critical point dryer (CPD).

The electrodes are connected to an external bias pad (not shown in Fig. 1) using a high-resistivity SiCr bias line. In order to save space, only one bias line and bias pad is used and the two electrodes are connected by a resistive line running underneath the CPW center conductor and covered by 2000 Å of $Si_xN_y$. This configuration turns out to be detrimental in terms of loss due to the high capacitance between the center conductor and the underlying resistive line.

Three different varactors ($C_1$, $C_2$, $C_3$) have been fabricated and measured with a bottom electrode width of 40, 70 and 120 $\mu$m respectively, in order to achieve three different capacitance values. Fig. 3(a) shows the equivalent model of varactor $C_2$. It is composed of an RLC series circuit for the MEMS bridge, and an RC series circuit representing the parasitic coupling to the bias line. Also, the $t$-line sections model the line underneath the bridge ($G/W/G = 130/70/130\ \mu$m) and at the input/output ports ($G/W/G = 80/160/80\ \mu$m). The equivalent model for varactors $C_1$ and $C_3$ is similar but with different component values. The values of the lumped elements are chosen in order to fit the measured S-parameters and are summarized in Table I. The capacitance $C_{MIM}$ represents the coupling capacitance between the CPW center conductor and the bias resistor, and is estimated from the parallel-plate formula ($C = \epsilon_0 \epsilon_r W w/g$) with $Si_xN_y$ ($\epsilon_r = 7.6$, $g = 2000$ Å). This coupling is fairly large and dominate the loss mechanism in the up-state and up to 15 GHz in the down-state. The losses, modeled by $R_s$ and $R_b$, are easy to extract by fitting the transmission coefficient ($S_{21}$). The capacitance ratio achieved

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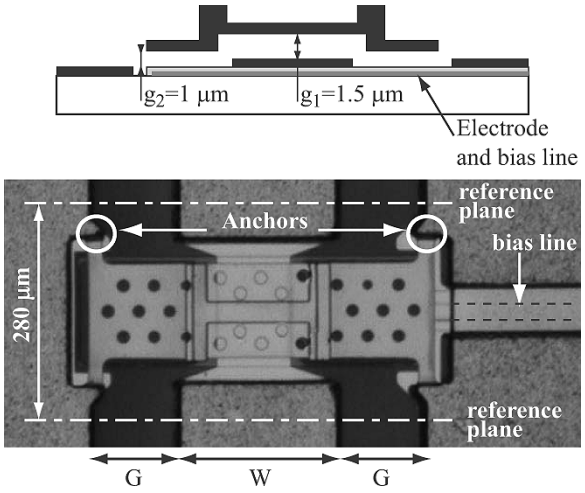


Fig. 1. Side view and top view of a discrete-position varactor on a CPW line ($G/W/G = 80/160/80\ \mu$m).

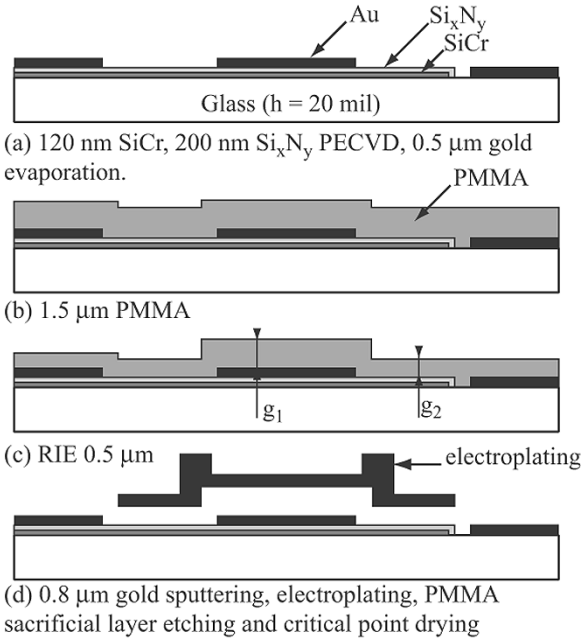


Fig. 2. Fabrication process of the discrete-position varactor.

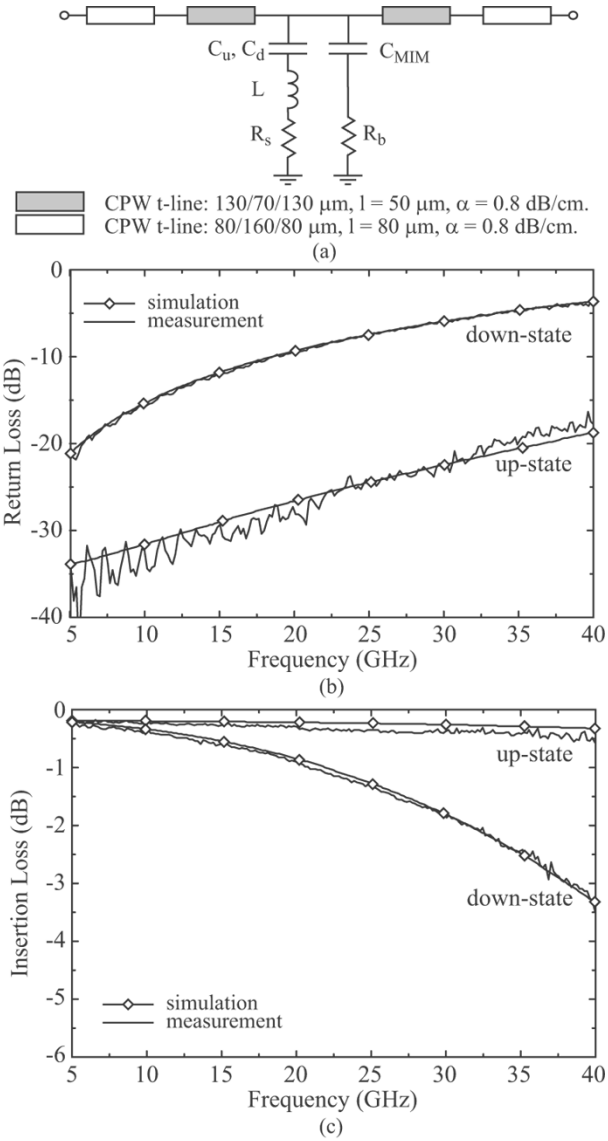


Fig. 3. Equivalent model of the varactor (a); $C_{MIM}$ and $R_b$ represent the parasitic coupling to the bias line (see Table I for component values). Measured and simulated return loss for varactor $C_2$ (45–145 fF) in up- and down-state positions (b).

TABLE I
VARACTOR MODEL: LUMPED-ELEMENT VALUES OF $C_u$, $C_d$, $C_{MIM}$ ($R_s = 1.5\ \Omega$, $L_s = 20$ pH, $R_p = 1300\ \Omega$)

| | $C_1$ | $C_2$ | $C_3$ |
|---|---|---|---|
| $C_u$ (fF) | 63 | 45 | 38 |
| $C_d$ (fF) | 205 | 145 | 80 |
| Cap. Ratio $C_d/C_u$ | 3.25 | 3.22 | 2.1 |
| $C_{MIM}$ (fF)* | 580 | 340 | 200 |

* estimated value

for varactors $V_1$ and $V_2$ is close to 3.25 while it is only 2.1 for $V_3$. This is due to the steps in the membrane which are located close to the center and cause some bending in the bridge. The pull-down voltage is around 15 V for all three varactors.

## III. 3-Bit Varactor Bank: Design and Measurements

The varactors presented above have been used to design a 3-bit varactor bank, composed of three discrete-position varactors placed in parallel across the CPW line (Fig. 4). Fig. 5 presents the measured reflection coefficient of the varactor bank for each state, and the extracted total capacitance value (146–430 fF). As expected, the overall capacitance ratio is 1 : 3 and is similar to the capacitance ratio of the individual varactors. The capacitance values (146–430 fF) are practical at X to Ku-Band since they correspond to an impedance $X = -j109$ to $-j37\ \Omega$ at 10 GHz. The same total capacitance is achieved in state 4 and 5. This is consistent with the extracted capacitance of the individual varactors shown in Table I, i.e., $C_{u1} + C_{d2} + C_{d3} = 63 + 145 + 80 = 288$ fF (state 4) and $C_{d1} + C_{u2} + C_{u3} = 205 + 45 + 38 = 288$ fF (state 5). A better choice of the individual capacitance values would provide eight truly different states.

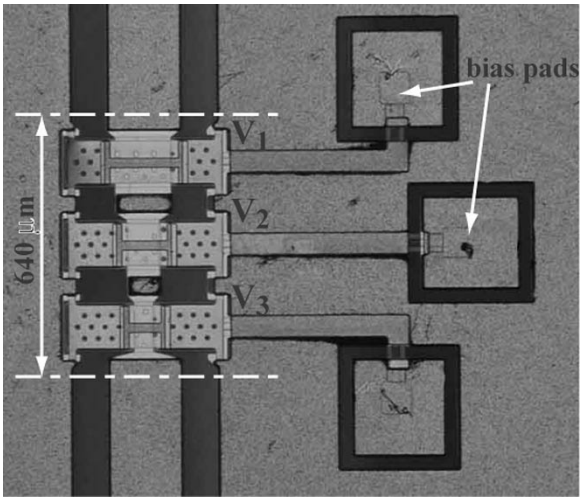


Fig. 4. Top view of the 3-bit varactor bank.

The frequency limitation of this circuit results from the t-line sections and added inductance between the varactors. The resonance frequency can be found by measuring the varactor bank on an open-circuited line and is defined as the frequency for which the reactive part of the impedance is null. The varactor bank achieved a resonance frequency of 25–36 GHz (state 8-state 1). The measured resonant frequency is 2–3x higher than the operating region of the 3-bit varactor. The design can be scaled to K-band by using a shorter spacing between the bridges to achieve a smaller inductance, and narrower membranes to get smaller capacitance values.

As explained in Section II, the measured quality factor is low ($Q = 5$–$10$ at 10 GHz), and this is due to the strong coupling to the bias line running underneath the CPW central conductor. Using the circuit model of Fig. 3, we can remove the effect of this coupling and take into account only the losses in the series resistance of the bridge ($R_s = 1.5\,\Omega$) and the simulated $Q$ is then 36–132 at 10 GHz. This is expected since this varactor has a Metal-Air-Metal configuration (no dielectric) at the capacitance location, and excellent performances have been reported in [3] with a varactor $Q$ of 100 at 34 GHz ($C = 80$ fF).

## IV. Conclusion

This paper presents the design, fabrication and measurement of a 3-bit digital varactor bank for X- to Ku-band operation. The circuit is composed of three different discrete-position varactors and covers a capacitance range of 146–430 fF. The quality factor of the varactor bank was low, due to an incorrect electrode connection design, but this type of component has already demonstrated very low losses in a previous design [3].

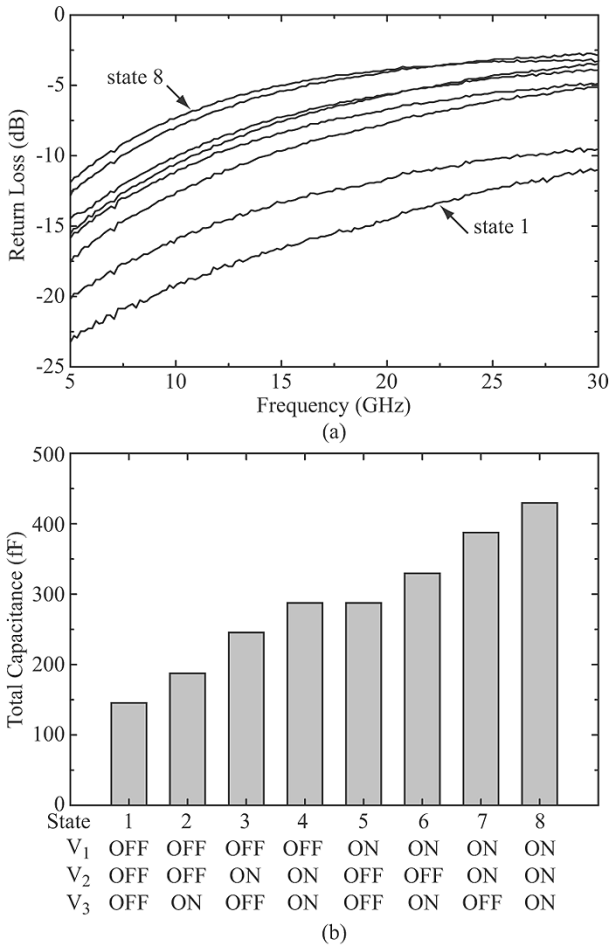


Fig. 5. Measured return loss for the 8 states of the 3-bit varactor bank (a) and capacitance value for each state (b) (OFF = up-state, ON = down-state).

Similar varactor banks are expected to have applications in millimeter-wave VCO's or tunable networks as they constitute very low loss and highly linear tuning elements.

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